A Novel Three-Phase Software Phase-Locked Loop

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***Abstract*—This paper describes the development of a novel three-phase phase-locked loop (PLL) used to compensate for mains variations by being incorporated as part of a feedforward loop in a three-phase telecommunications power converter. A telecommunications converter must comply with industry standards, in particular the psophometric noise standard CCIF-1951; this is achieved by controlling the output voltage ripple from the dc-dc converter. It is required that psophometric compliance is maintained under expected mains variations documented in the EN50160 power quality standard. The software PLL is simulated and performance characteristics show a high degree of noise rejection while also maintaining good dynamic performance.**

I. Introduction

A new three-phase single-stage converter has been proposed [1]. These converters are manufactured for the telecommunications industry and as such need to conform to certain standards. The major ones are the CCIF-1951 standard, commonly called the psophometric standard, and the IEC1000-3-2 harmonic standard. The IEC1000-3-2 standard was introduced to regulate the harmonic currents drawn from the mains. Compliance with this standard is achieved by using active power factor correction techniques.

Telephone networks were originally analogue and because of output voltage ripple coming from the converter, audible noise was produced on the phone lines. Nowadays, with digital exchanges the telephone systems have become immune to dc power supply noise. The psophometric standard is still used however as the defining standard for the interface between telecommunication switching equipment and telecommunication dc power equipment.

This new design of converter achieves compliance by allowing constant three-phase power to flow from the source to the load by implementation of a squaring transfer function on the input voltages [1]. This action allows the load to be ripple free, as well as providing power factor correction. Given that the IEC1000-3-2 standard only needs to be met under nominal mains conditions, no further engineering effort is required with the design as compliance is virtually guaranteed. However, even under nominal operating conditions the psophometric standard will not be met due to the new converter design relying on the requirement that the three input phase voltages are balanced with equal magnitudes at all times in order to obtain zero output voltage ripple.

In order to theoretically maintain zero output voltage ripple a three-phase PLL is needed as a feedforward loop in order to compensate for mains variations between phases [1]. The PLL outputs serve as a reference; since it is synchronized with the mains, the outputs represent ideal mains voltages. Any discrepancies between the PLL outputs and the actual mains voltages then show up as an error signal that is fed forward with the converter controller generating the appropriate compensation signals used to maintain a constant power flow to the load. This prevents any voltage ripple due to mains amplitude variations from occurring [2].

A novel PLL design has been proposed in [2] and unlike the traditional three-phase PLL this new design involves no coordinate transformations, resulting in a more simple design that is computationally more efficient. Fig. 1 shows the PLL system.

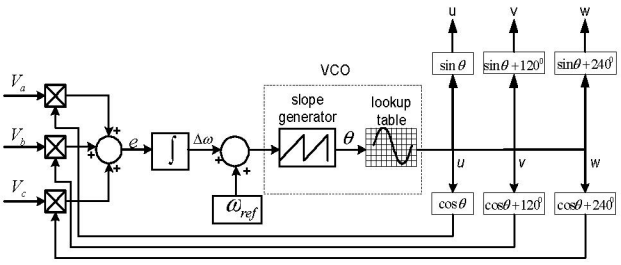

Fig. 1. Novel PLL Structure

It can be seen that the main difference between this new PLL compared with the traditional three-phase PLL is that there are no coordinate transformations and that the three phase detectors (multipliers), have their outputs summed together. This has the effect of cancelling the second harmonic signal, which is always present in single-phase PLL systems, as well as cancelling any common phase noise, thus reducing the overall filtering effort required [2]. Summing together the three phase detector outputs result in a dc error signal e. Elimination of the error signal is achieved by changing the phase of the feedback signals (u,v,w) to match the phase of the input voltages (V_a,V_b,V_c). The voltage-controlled oscillator (VCO) performs this task. If the error signal is zero the VCO produces a 50Hz quiescent frequency ω_{ref}, but if the error signal is a non zero value, then it responds by adjusting its operating frequency until a phase lock is achieved.

II. Software PLL Operation and Modelling

A. Operational Principle

The three-phase PLL software model is shown in Fig. 2.

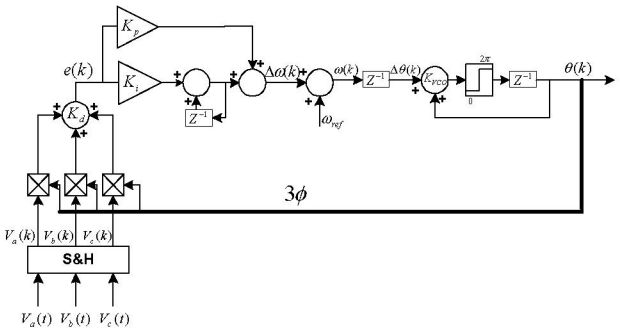

Fig. 2 Software PLL Model

The three-phase inputs after being sampled by the digital signal processor (DSP) are represented as

$$V_a(k) = 1PU\sin(\theta(k))$$
$$V_b(k) = 1PU\sin(\theta(k) + 2\pi/3)$$
$$V_c(k) = 1PU\sin(\theta(k) - 2\pi/3)$$

The multipliers serve as phase detectors, with the phase error in each phase being summed together resulting in a dc error signal *e(k)*. This error signal is fed into the proportional-integral controller of the PLL and used to calculate the change in angular frequency of the mains voltage $\Delta\omega(k)$.

$$\Delta\omega(k) = \left(K_p + \frac{K_i z}{z-1}\right)e(k)$$

The reference angular frequency $\omega_{ref}=2\pi f$ (where f is the reference frequency 50Hz), is added to $\Delta\omega(k)$.

$$\omega(k) = \Delta\omega(k) + \omega_{ref}$$

Multiplying $\omega(k)$ by the sampling time, which is represented by unit delay z^{-1}, determines the sampling time increment of the phase angle $\Delta\theta(k)$.

$$\Delta\theta(k) = z^{-1}\omega(k)$$

Integrating the increment $\Delta\theta(k)$ over the range 0-2π the estimated phase angle of each three-phase mains phase voltage $\theta(k)$ is obtained.

$$\theta(k) = \frac{z\Delta\theta(k)}{z-1}$$

The estimated angle is fed back into the phase detectors and used to adjust the error signal towards zero, resulting in the estimated angle and the grid phase angle being the same.

B. Modelling

By assuming the phase error is kept within a limited range, the PLL can be modelled as a linear system. This is a reasonable assumption since PLLs are normally only operated within their locking range, as beyond this range instability results [3]. A linear discrete model based on sampled data is shown in Fig. 3.

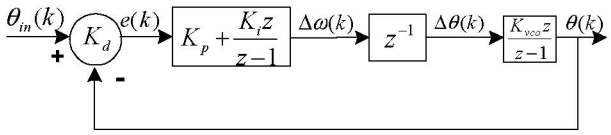

Fig. 3 Linear Discrete Software Model

In Fig. 3, as in Fig. 2, K_p and K_i represent the proportional and integral gains and z^{-1} represents a sample delay. In addition, K_d is the phase detector gain; it determines the phase detector output in response to a phase error. K_{vco} is the gain of the VCO. For equation simplicity we set $K_{vco}K_dK_p=\alpha$ and $K_{vco}K_dK_i=\beta$, and the closed loop transfer function of Fig. 3 can now be written as

$$\frac{\theta(z)}{\theta_{in}(z)} = \frac{(\alpha+\beta)z - \alpha}{z^2 + (\alpha+\beta-2)z + (1-\alpha)} \quad (1)$$

C. Loop Stability

A digital PLL is stable if all of its poles are inside the unit circle and unstable if any pole lies outside the unit circle. One of the most efficient criteria for testing the stability of a discrete-time system is Jury's stability criteria [3]. For a second order system, according to this criterion, the conditions for stability are

$A(1)>0$
$A(-1)>0$
$|k_0|<k_2$

where A is the denominator of the transfer function, which can be rewritten as

$$A(z)=k_2 z^2+k_1 z+k_0=0$$

applying these conditions stability is obtain when

$0<\alpha<2$ and $0<\beta<4$

D. Steady State Phase Error

Consider a step change in the phase of the incoming signal, which can be shown as

$$\theta_{in}(t) = u(t)\Delta\theta_{in}$$

$u(t)$ is the unit step function and $\Delta\theta_{in}$ is the size of the input phase step. The instantaneous phase has jumped from its old value to a new value by $\Delta\theta_{in}$. In the z domain this can be expressed as

$$\theta_{in}(z) = \frac{\Delta\theta_{in} \bullet z}{z-1}$$

and the phase error transfer function E(z) for a digital system can be expressed as

$$E(z) = \left[1 - \frac{\theta(z)}{\theta_{in}(z)}\right]\theta_{in}(z)$$

substituting (1) into E(z) gives

$$E(z) = \frac{\Delta\theta_{in} \bullet z(z-1)}{z^2 + (\alpha+\beta-2)z + (1-\alpha)}$$

Applying the final value theorem to E(z)

$$\lim_{k\to\infty} e(kt) = \lim_{z\to 1} \frac{\Delta\theta_{in}(z-1)^2}{z^2 + (\alpha+\beta-2)z + (1-\alpha)}$$

Setting z=1 it can be seen that the expression becomes zero, thus proving that the error signal over time will go to zero in response to a step phase change at the input. Further analysis shows similar results under conditions of a frequency step and a frequency ramp [4].

E. Coefficient Determination

To fully make use of the transfer function one needs to determine the relevant gain coefficients. The phase detector gain is the slope of the output calculated as cycles^{-1}. This was determined to be K_d=0.978cycles^{-1}. The VCO gain is the change in output frequency in response to an error signal, this was calculated to be K_{vco}=0.099cycles (see Appendix). To check the validity of these coefficients a cross check against expected values, based on the performance of the PLL, has been carried out. Setting K_p=0.0625 and given the following equation:

$$|\Delta f_l| = f_s K_{vco} K_d K_p \tag{2}$$

where f_s=sampling frequency and f_l=lock range

It was found that the lock range extended from 45Hz to 54Hz and since f_s=10kHz, Δf_l=9Hz and K_p=0.0625 the product $K_{vco}K_d$ was found to be 0.09 from (2). The same product, using analytical techniques described in the Appendix was found to have a value of 0.089. Therefore, these results give confidence that the calculated values are a fair reflection of the actual PLL internal system gains.

III. Performance Criteria

The desired performance of the PLL can now be implemented by adjusting the proportional and integral gains. A system that has a high bandwidth, although good for initial locking, does tend to enhance voltage distortions on the output [5]. Bandwidth is therefore a tradeoff between the filtering performance and the response time. The larger the bandwidth the better the response times, but the poorer the filtering action.

According to the European power quality standard EN50160, which provides the limits and tolerances of various phenomena that can occur on the mains, it is expected that the mains frequency may deviate by up to ±1Hz. Frequency can be represented as a change in phase angle over time given by the expression

$$\omega(t) = \frac{d\theta}{dt}$$

therefore, a ±1Hz grid frequency deviation is simply a change of 2π radians or 360° per second.

$$\frac{\Delta\theta}{\Delta t} = 2\pi$$

The required time for the mains to reach its steady state is now

$$\Delta t = \frac{\Delta\theta}{2\pi} \tag{3}$$

According to[6], dips in transmission services result in phase angle jumps of approximately ±5° or 5π/180. Substituting into (3), results in a settling time of 13.8ms.

The following time continuous approximations can be made for a digital system as discussed in [4].

$$\varsigma \approx \frac{1}{2}\sqrt{\frac{K}{K_i}} \tag{4}$$

$$\omega_n \approx f_s\sqrt{KK_i} \tag{5}$$

where

f_s= sampling frequency
K=loop gain= $K_dK_{vco}K_p$
ζ=damping factor
ω_n=natural frequency

The PLL is chosen to have a damping factor of 0.707 as this should allow only one overshoot in the transient response and it is well known to be the optimum damping factor value. Choosing values of K_p=1 and K_i=0.045 will give ζ=0.707 according to (4). Applying these values as well as the known values for K_{vco} and K_d to the transfer function in (1) gives the following closed loop transfer function:

$$H(z) = \frac{0.094z - 0.09}{z^2 - 1.906z + 0.91} \tag{6}$$

IV. Simulation

The transfer function in (6) has been simulated using a software package called PSIM. The input step response and the frequency and phase responses are shown in Figs. 4 and 5 respectively.

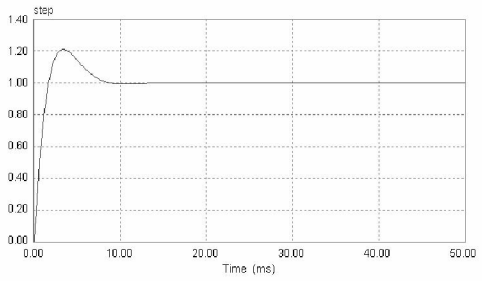

Fig. 4 PLL Input Step Response

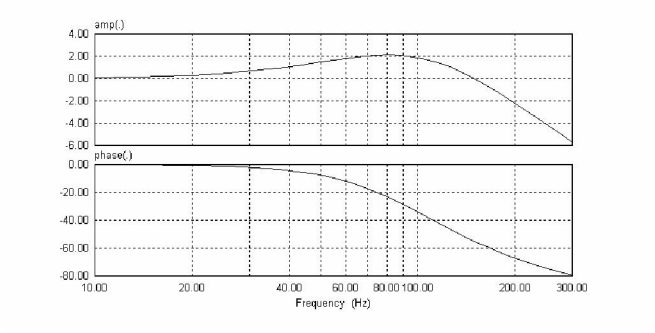

Fig. 5 PLL Frequency and Phase Response

From the simulations, it can be seen that the input step response (Fig. 4) yields a settling time of 8ms. The frequency response plot of gain (decibels) vs frequency (Hertz) (Fig. 5) shows that the PLL has a natural frequency of 149Hz, while (5) approximates to 121Hz. The phase response (Fig. 5) shows the phase angle (in degrees) vs frequency. The system is shown to have a phase margin of 126° and a gain crossover frequency of -54° indicating a stable system.

It can also be seen from the frequency response graph that there is some gain peaking. This is due to the fact that there is always a zero in the numerator of the transfer function even though the spacing between the zero and the closest pole decreases with increasing damping, but the pole never actually coincides with the zero therefore a second order PLL will always exhibit some peaking.

V. Software PLL Performance

A. PLL Experimental Setup

The proposed PLL technique is implemented using the DSP TMS320F2812. Some of the main features of this DSP are a 150MHz clock, analogue to digital converters (A/D) with 12-bit resolution and six PWM output ports [7]. Fig. 6 shows the experimental setup for the PLL. A three-phase function generator produces the mains voltages. The on-board A/D converters sample these input signals and consequently the PLL outputs the generated phase signals via the PWM ports. The outputs go through low pass filtering to remove the high frequency PWM switching harmonics.

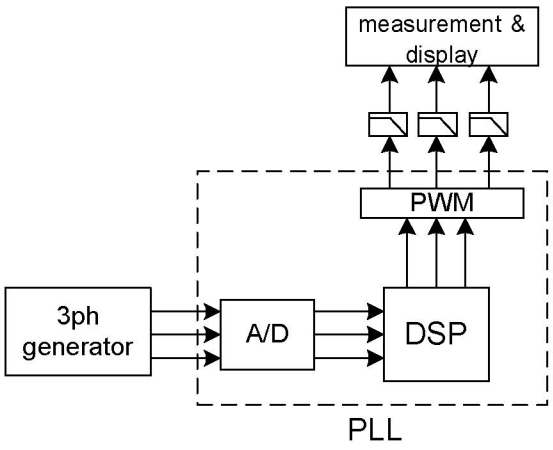

Fig. 6 Experimental Setup for PLL System

B. PLL Transient Response

The PLL is started up while the three-phase generated mains applied to the inputs and the response of the red phase is shown in Fig. 7. The PLL at startup has a 180° phase shift with respect to the input phase voltage and phase lock is achieved within 10ms.

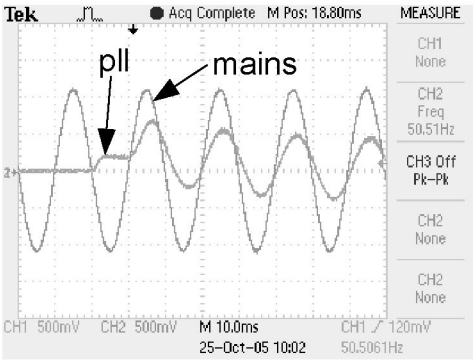

Fig. 7 PLL Startup Response

In Figs. 8 and 9, the PLL undergoes phase angle jumps. This is easier to perform than a phase jump on one phase of the function generator and yet achieves the same effective outcome of determining how well the PLL copes with a sudden phase angle change. A phase jump is achieved by resetting the VCO at the appropriate time. The response of the PLL to a phase angle jump of 90° is shown in Fig. 8 and it can be seen that the PLL is able to recover from the disturbance and regain tracking after 7ms. Fig. 9 shows that in the worst case, a 180° phase angle jump, the PLL regains synchronism in 10ms. The PLL output signals are generated by the PWM ports. Therefore, in order to see the output waveforms the PWM signals need to be filtered to remove the switching harmonics. As a consequence of passing the signals through a passive low pass filter, there is a phase shift introduced, hence the apparent phase shift between the mains and the PLL outputs.

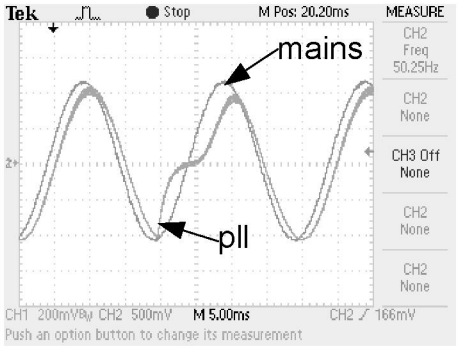

Fig. 8 PLL Under 90° Phase Angle Jump

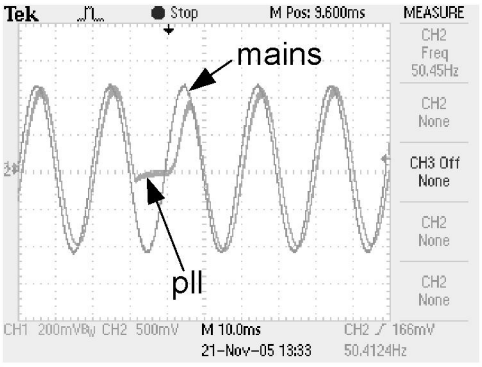

Fig. 9 PLL Under 180° Phase Angle Jump

C. *PLL Under Distorted Mains*

In reality the mains voltage is not a pure sinusoid but can be distorted by various non-linearity's such as phase imbalances and line harmonics.

In figures 10 and 11 the PLL output is shown under various three-phase mains distortions. The figures show a single phase input and corresponding output, however the waveforms are the same for all three phases.

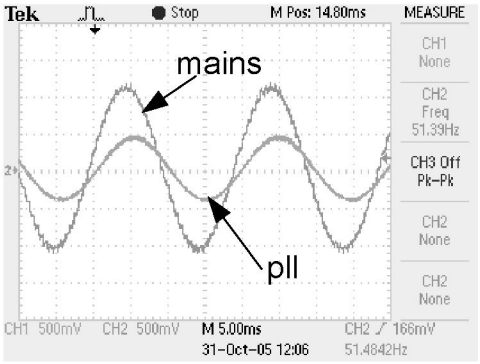

Fig. 10 Mains With Added Noise

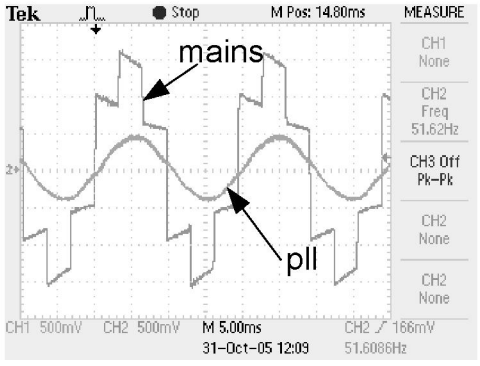

Fig. 11 Mains With Severe Harmonic Distortion

What can be seen from the waveforms is the ability of the PLL to maintain phase lock under distorted conditions. This is because the input phases are summed together resulting in a cancellation of all common phase distortions.

D. *Magnitude Imbalance*

Introducing a phase imbalance, which can be seen in Fig. 12, a phase is attenuated by 10%, the expected maximum phase sag according to the EN50160 power quality standard. Applying this phase imbalance to the PLL results in the PLL obtaining phase lock, the results of one phase are shown in Fig. 13.

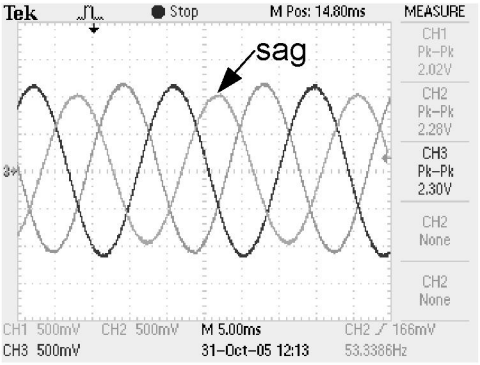

Fig. 12 Mains Phase Imbalance

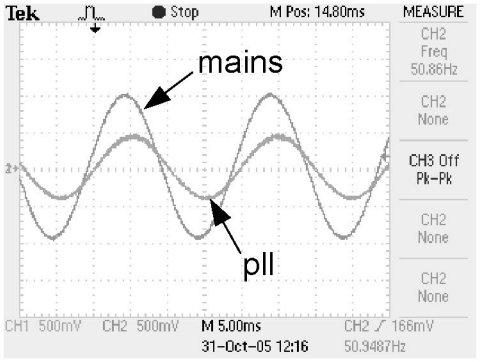

Fig. 13 PLL Output Under Phase Imbalance

VI. Conclusion

A novel software three-phase PLL has been introduced and a system model transfer function derived. Analysis has determined that for the particular application of the PLL used to monitor mains variations, the maximum required synchronisation time for the PLL after a phase angle disturbance is no more than 13.8ms.

Simulations of the transfer function transient response show a settling time of around 8ms with one overshoot. Simulations also show a natural frequency of 149Hz with a phase margin of 126° thereby indicating that the PLL is inherently stable.

The PLL was implemented on a DSP and the results show a worst-case 10ms synchronisation time in response to a phase angle jump. Under distorted mains conditions the PLL was shown to be able to maintain phase lock and produce a clean output waveform.

The PLL has been demonstrated to have a very good filtering action with the ability to naturally remove all common phase distortions; this allows the PLL system to have both excellent noise rejection and a high degree of robustness.

ACKNOWLEDGMENT

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APPENDIX

The phase detector gain K_d is determined by analysing the slope of the phase detector. The linear approximation of the phase detector is shown in Fig. 14.

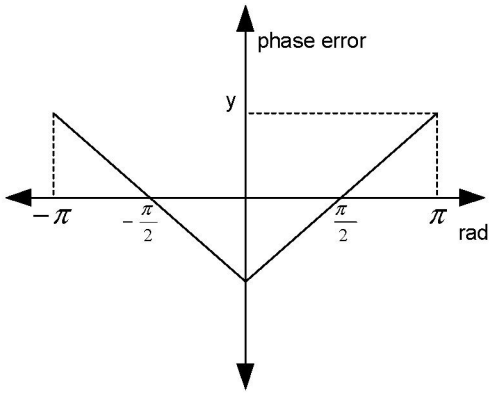

Fig. 14 Phase Detector Output

From empirical measurement y=24564 and the slope of the phase detector K_d is calculated as

$$K_d = \frac{24564}{\pi/2}$$

$$= 15638 rad^{-1}$$

Since the sampling frequency is 10kHz and the phase detector has the range $-\pi$ to π the number of cycles per radian is 15708. Therefore

$$K_d = \frac{15638}{15708}$$

$$= 0.978 cycles^{-1}$$

The VCO gain K_{vco} is calculated by determining the output of the VCO in response to an error signal. The VCO concerned has a $0.063 rad.s^{-1}$ change in frequency in response to the smallest error signal. Therefore

$$K_{vco} = \frac{0.063 rad.s^{-1}}{10 kHz}$$

$$= 6.3 \times 10^{-6} rad$$

Since the VCO generates a slope over the range 0-2π and with the sampling frequency of 10kHz, the VCO cycles are calculated as

$$= 6.3 \times 10^{-6} rad \times 15708 \ cycles.rad^{-1}$$

$$= 0.099 cycles$$